Designing Converters with the NCP101X Family

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APPLICATION NOTE

For moderate power offline applications, a monolithic circuit, such as the NCP101X series, represents a pertinent choice for engineers looking for design speed and ease of implementation. Incorporating everything needed to build reliable and safe Switch−Mode Power Supplies (SMPS), the NCP101X combines a current−mode controller and a 700 V power MOSFET. Due to ON Semiconductor proprietary high−voltage technology, the device directly supplies itself from the rectified mains and, in numerous cases, does not need an auxiliary winding to operate. This application note details the internal circuit operation and gives tricks to make your design successful.

The Specs at a Glance

The NCP101X capitalizes on the successful NCP1200 series where the words *compactness* and *flexibility* could both be applied to qualify the controller philosophy. In this particular version, the controller looks very similar to that of the 1200 but a 700 V lateral MOSFET has been added to the part. Let's quickly browse its features:

- **No Need of Auxiliary Winding:** ON Semiconductor's Very High Voltage Integrated Circuit technology lets you supply the IC directly from the high−voltage DC rail. We call it Dynamic Self−Supply (DSS) and was already implemented in the 1200 series. This solution simplifies the transformer design and ensures a better control of the SMPS in difficult output conditions, e.g. constant current operations or overload. However, for improved standby performance, an auxiliary winding can be connected to the Vcc pin to disable the DSS operation.
- **Short−Circuit Protection:** By permanently monitoring the feedback line activity, the IC is able to detect the presence of a short−circuit, immediately reducing the output power for a total system protection. Once the short has disappeared, the controller resumes and goes back to normal operation.
- **Fail−Safe Optocoupler and OVP:** When an auxiliary winding is connected to the Vcc pin, the device stops its internal Dynamic Self−Supply and takes its operating power from the auxiliary winding. An 8.7 V active clamp is connected between Vcc and ground. In case the current injected in this clamp exceeds a level of around 7.4 mA typ., the controller immediately latches off and stays in this position until the user cycle Vcc down to 3.0 V (e.g. unplugging the converter from the wall). By adjusting a limiting resistor in series with the Vcc terminal, it becomes possible to implement an over voltage protection function, latching off the circuit in case of broken optocoupler or feedback loop problems.
- **Low Standby−Power:** If SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping unneeded switching cycles, the NCP101X drastically reduces the power wasted during light load conditions. An auxiliary winding can further help decreasing the standby power to extremely low levels by invalidating the DSS operation. In that case, experience shows that a standby power below 100 mW at 230 VAC is achievable.
- **No Acoustic Noise While Operating:** Instead of skipping cycles at high peak currents, the NCP101X waits until the peak current demand falls below a fixed 1/4 of the maximum limit. As a result, cycle skipping can take place without having a singing transformer. You can thus select cheap magnetic components free of noise problems.
- **SPICE Model:** A dedicated model to run transient cycle−by−cycle simulations is available but also an averaged version to help you closing the loop. Ready−to−use templates can be downloaded in OrCAD's PSpice, and INTUSOFT's IsSpice4 from ON Semiconductor's web site, NCP101X related section.

October, 2003 − Rev. 0
Publication Order Number:
AND8134/D

The Dynamic Self−Supply

A Dynamic Self−Supply (DSS) offers an easy means to provide power to the control section, without using an auxiliary winding. The DSS consists in a current source connected to the swinging high−voltage drain, and operated *on* or *off* depending on the Vcc level: if the Vcc is below a given value, the source is *on* and Vcc rises up. When Vcc has reached the desired value, the source turns *off*, and no longer consumes power. This system is self−regulated and works as a hysteretic regulator: if the consumption increases, the current source will stay *on* longer and the *off* period will shorten. As a result, the DSS being connected to the drain, the *average* current taken from that path, reflects the average current drawn from the Vcc pin (neglecting the DSS operation losses). Figure 1 depicts the way the DSS is implemented and Figure 2 portrays its typical operating signals.

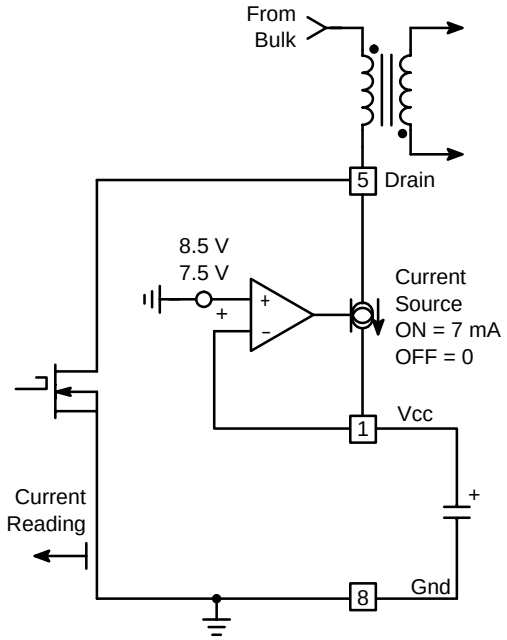

Figure 1. The internal supply implementation . . .

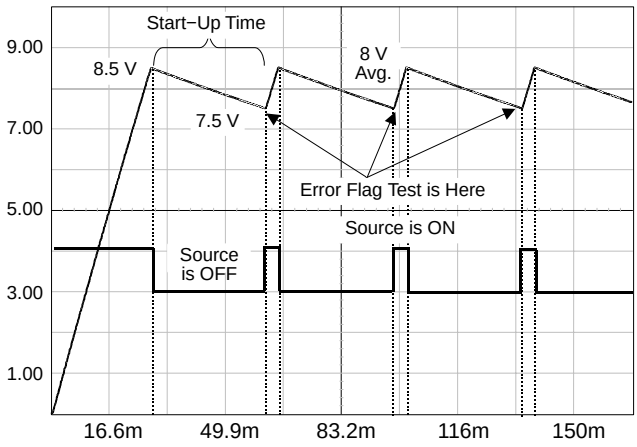

Figure 2. . . . and its typical operating signals, like the Vcc ripple.

The DSS up and down slopes are internally used as timers to eventually detect an error condition, e.g. an overload event. When the feedback level is pushed to the maximum, an active clamp starts to operate and limits the current, cycle by cycle. This active clamp is nothing else than the usual 1.0 V “zener” you find in the NCP120X series, except that the clamping level is smaller in the NCP101X series. As soon as this clamp is activated, it asserts a digital flag, testifying for an overload condition or a loss of the feedback signal. When the Vcc logic senses that 7.5 V is reached AND that the error flag is asserted, the logic stops pulses and enters a safe, auto−recovery, burst mode. As soon as the error goes away, the SMPS resumes its operation.

Overload events always happen during the start−up sequence where the controller strives to grow Vout. During that time, the loop pushes the peak current to the maximum (hence the clamp activation) and waits until Vout reaches the target. The time given by the controller to let the supply build−up Vout corresponds to the *first* downslope (see Figure 2). If the error flag is still high at the first 7.5 V event, then the controller activates the burst. As a result, it is important to check with the oscilloscope that the device regulates before the first 7.5 V event. This can be done by monitoring the FB pin (pin4) and the Vcc pin (pin1). As Figure 3 indicates, a proper dimensioning of CVcc implies a FB release before the end of the downslope.

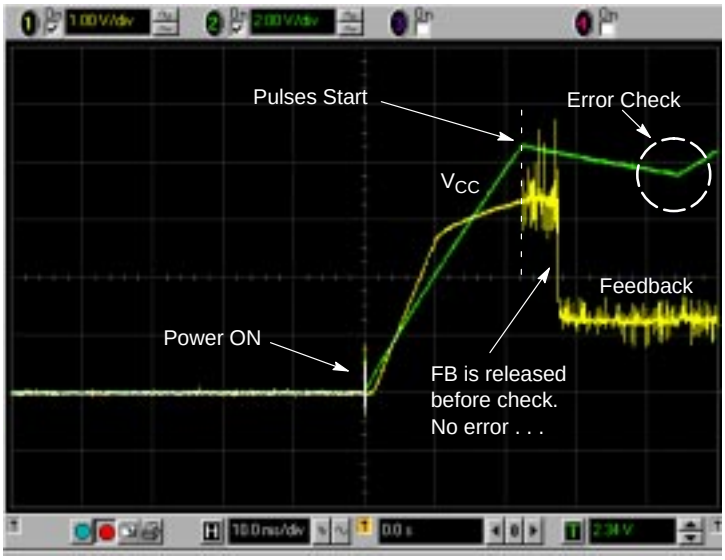

Figure 3. The release of the FB pin before the first 7.5 V event indicates that the supply has enough time to start−up.

EMI Jittering Using the Vcc

The ripple excursion that you notice on the Vcc is internally used to modulate the switching frequency of the PWM controller. Typically, a 3.3% deviation is observed for a Vcc sweep between VccON and VccOFF, e.g. 62.8 kHz @ 7.5 V up to 67.2% @ 8.5 V typically for a 65 kHz reference. This so−called frequency jittering lowers the EMI peaks at Fsw and its following harmonics.

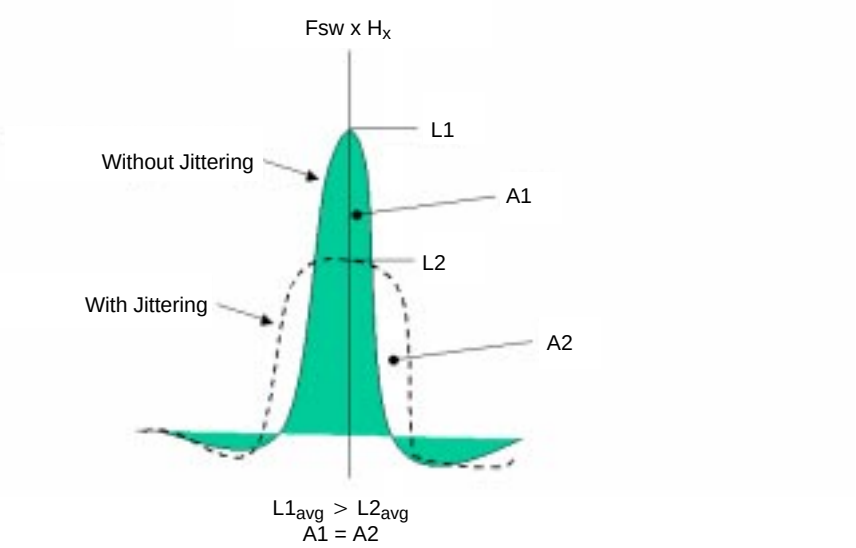

Figure 4. Frequency Jittering Spreads the Energy Content and Lowers Discrete Peaks

The jittering actually performs a so−called spread spectrum modulation which “spreads” the energy to adjacent frequencies rather than inside a single ray. When the EMI receiver opens it’s narrow filter window at a given frequency F1, the accumulated (averaged) energy at F1 is reduced by the low frequency modulation. As a result, less efforts are needed on the input filter design.

Connecting an auxiliary winding to the Vcc disables the frequency modulation since the DSS ripple fades away.

The DSS and the Duty−Cycle

In the NCP101X series, the current source is connected to the drain node, unlike the 120X family where it was tied to the DC bulk rail. As a result, the current source “sees” a swinging node affected by a large dV/dt with voltage excursions from almost ground (MOSFET is ON) up to nearly 700 V (MOSFET is OFF). This situation can sometimes affect the DSS behavior, especially if the duty−cycle exceeds 45%. In that case, the voltage necessary to operate the source is too low and the available current cannot refuel the Vcc capacitor. Why, since the average voltage across Lp being null, the current source should face a similar situation as when connected to the bulk? In reality, the pulse frequency makes the situation difficult for the current source, a high−voltage MOSFET, that needs to be quickly turn−on during the OFF time only. At a certain point, if the duty−cycle is too large, the DSS voltage starts to bend before stopping its hysteretic regulation. Figure 5 portrays typical curves where the duty−cycle expands toward 50% and engenders the DSS bending. Should the duty−cycle further increase, the DSS would stop (the Vcc simply flattens) but the IC would still continue to operate.

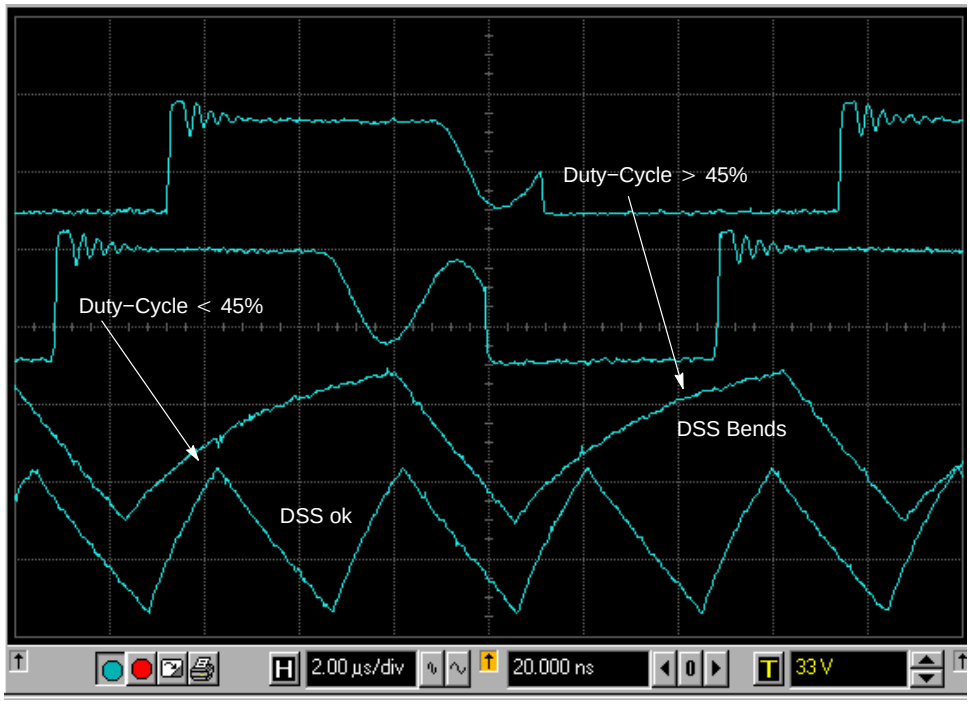

Figure 5. When the duty−cycle exceeds 45%, the DSS starts to bend, indicating the beginning of the limit for the DSS.

To take the full benefit of the DSS, here are some recommendations that need to be understood for a successful design:

- Design for a steady−state duty−cycle smaller than 45% at minimum input voltage and maximum load. It is not a problem that *transient* duty−cycles exceed that limit, e.g. during load variations. The NCP101X can work in both DCM and CCM without problem.
- If necessary, grow−up the bulk capacitor to reduce the ripple at low line and thus increase the available rectified DC voltage in worse input case.

Be sure to test your final design at the right ambient temperature while observing the Vcc ripple. A slightly bent ripple as on Figure 4 is not a problem if observed at high ambient temperatures.

DSS or Auxiliary Winding?

The DSS being directly connected to the drain node, its power dissipation can sometimes affect the remaining heat dissipation room of the MOSFET if the DSS power budget is too high. Since the average voltage across the transformer primary inductance is null at steady−state, the average power taken by the DSS to supply the controller is: Vbulk x ICC1, neglecting switching losses. If Vbulk is 370 V and ICC1 roughly 1.0 mA, then the DSS power is already 370 mW. Suppose our package can dissipate 930 mW @ 50°C $T_{AMBIENT}$, then the room left for the MOSFET is only 930m–370m = 560 mW, naturally hampering the power capability of the considered device. Also, the no−load standby power cannot be lowered below these 370 mW at high line since the DSS is always operating. A solution to improve the situation could be to disable the DSS by an auxiliary winding and reduce the power drawn by the controller to almost nothing. This improves the no−load standby power and the 100 mW barrier is in sight. Also, the package power dissipation becomes entirely dedicated to the MOSFET alone, considerably raising the power capability of the considered device. So, when using an auxiliary winding or the Dynamic Self−Supply?

- You need an extremely low standby power: use an auxiliary winding
- You design a low power converter < 5.0 W: DSS is okay
- EMI filtering is a sensitive issue, you need jittering: use DSS
- You want to pass the maximum power from a NCP101X member: use an auxiliary winding
- A precise short−circuit protection is a must: use DSS
- Safety motivates an open−loop protection: use an auxiliary winding

The Vcc Pin

The NCP101X features an active clamp on its Vcc pin: when the voltage presents on this pin exceeds VccOFF + 200 mV typical, a zener−like circuitry starts to activate and prevents the voltage from going further up. Of course, in DSS mode, this circuit is unactive since the current source stops the Vcc excursion at VccOFF. A circuit permanently monitors the current flowing in this zener circuit. When this current reaches a certain value (7.4 mA, typical), a comparator permanently latches−off the controller and the user must cycle the Vcc down to 3.0 V to reset the latch. As a result, when you connect an auxiliary winding, you MUST limit the current flowing into the Vcc pin otherwise a) you have risks to destroy the active zener if the injected current exceeds 15 mA b) you will latch your converter in off state as soon as it starts−up.

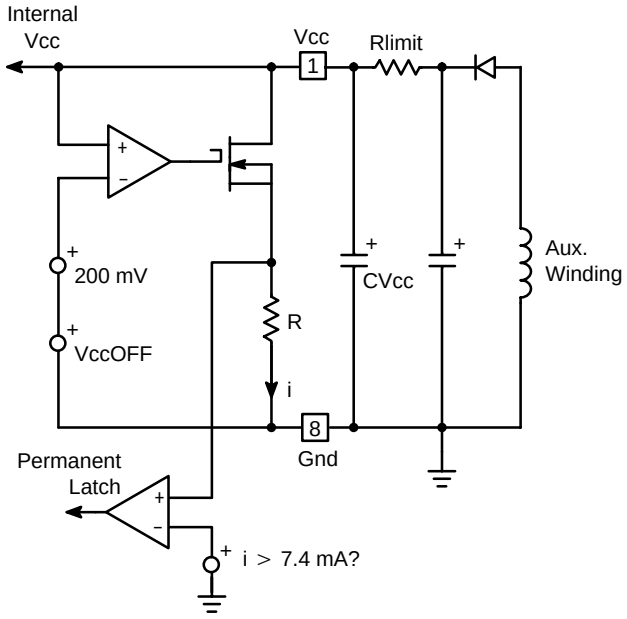

Figure 6. An active clamp limits the voltage excursion on the Vcc pin and triggers a latch if the injected current is too high.

This protective feature can be used to protect the load and the converter in case of broken optocoupler for instance. Calculating the Rlimit resistor is easy as long as one understands the particularity of a converter featuring an extremely low standby power.

Self−supplying controllers in very low standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (Vnom), this voltage can drop to below 10 V (Vstby) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency re−fueling rate of the Vcc capacitor is not enough to keep a proper auxiliary voltage. So care must be taken when calculating Rlimit to 1) not trigger the Vcc over current latch (by injecting 6.3 mA (minimum of the spec) into the active clamp) in normal operation but 2) not to drop too much voltage over Rlimit when entering standby. Otherwise the DSS could be kept deactivated and the standby performance would degrade. We are thus able to bound Rlimit between two equations.

$$\frac{Vnom - 8.7\ V}{Itrip} \leq Rlimit \leq \frac{Vstby - VccON}{ICC1} \quad \text{(eq. 1)}$$

Where:

Vnom is the auxiliary voltage at nominal load.

Vstdby is the auxiliary voltage when standby is entered.

Itrip is the current corresponding to the nominal operation. It thus must be selected well below 6.3 mA to avoid false tripping in overshoot conditions. We use the minimum value of the spec to cover all distribution cases from NCP101X lots to lots.

ICC1 is the controller consumption in skip mode. This number slightly decreases compared to ICC1 from the spec since the part in standby does almost not switch.

VccON is the level at which Vauxiliary must be maintained to keep the DSS in the OFF mode. It is good to shoot above 8.0 V in order to offer an adequate design margin, for instance 8.2 V. Also, we shall not trigger the active clamp too much otherwise the consumption will increase and standby power quickly degrades. When you try to pass the 100 mW barrier, every single milliwatt counts!

Since Rlimit shall not bother the controller in standby, e.g. keep Vauxiliary above 8.2 V (as selected above), we purposely select a Vnom well above this value. As explained before, experience shows that a 40% decrease can be seen on auxiliary windings from nominal operation down to standby mode. Let's select a nominal auxiliary winding of 20 V to offer sufficient margin regarding 8.2 V when in standby (Rlimit also drops voltage in standby). In that case, the current flowing through Rlimit will be ICC1 (the supply of the controller) + Iclamp, Iclamp circulating in the activated zener diode. If we select the NCP1013 operating at 65 kHz, ICC1 = 1.0 mA. Selecting a clamp current Itrip of 5.0 mA (to be below the 6.3 mA min. trip point) leads to a total current of 6.0 mA. Applying equation 1 gives:

$$\text{Rlimit} = \frac{20\ \text{V} - 8.7\ \text{V}}{6\text{m}} = 1.8\ \text{k}\Omega < \text{Rlimit}$$

$$< \frac{12\ \text{V} - 8.2\ \text{V}}{1\text{m}} = 3.8\ \text{k}\Omega$$

If we design a 12 V power supply, then the ratio between auxiliary and power must be: 12/20 = 0.6. The OVP latch will activate when the clamp current exceeds 6.3 mA, at the minimum of the spec. Theoretically predicting the auxiliary drop from nominal to standby is an almost impossible exercise since many parameters are involved, including the converter time constants. The fine tuning of Rlimit thus requires a few iterations and experiments on a breadboard to check Vauxiliary variations. Once properly adjusted, the fail−safe protection will preclude any lethal voltage runaways in case a problem would occur in the feedback loop. To fine tune Rlimit, please follow the steps:

1. Select the highest Rlimit value, e.g. 3.8 kΩ given by equation 1.
2. Remove the output load.
3. Connect a scope probe to the cathode of the auxiliary diode while observing the output voltage on another channel. Select one shot operation on the scope, with a positive trigger monitoring Vaux.
4. Power the converter with the maximum input voltage and short the optocoupler LED: Vaux grows−up until the IC latches−off. Capture a one−shot graph as on Figure 7, note Vout max and Vaux max. Vout has gone, the controller is latched. If not, reduce Rlimit and retry step 4 until it latches−off. To quickly reset the controller, do a brief short between Vcc and ground.
5. Stop the converter, and make sure Vout is back to zero.
6. Now, as detailed in step 3, capture a fresh start−up sequence and note Vaux max as in Figure 8.
7. If you have a sufficient margin between the auxiliary level overshooting at start−up (16 V in our case) and the level at which it latches−off (32 V in the example), then you have a safe design. If necessary, there is room to reduce Rlimit and thus decrease the latching voltage.
8. Check the standby power and the voltage on pin 1 during no−load and maximum input voltage. If Vpin1 is really close to 8.7 V in no−load conditions, there are chances that the clamp activates and increase the consumption. If you do not pass the 100 mW barrier, you can increase Rlimit to drop Vpin1 slightly below 8.7 V (or check that the watt−meter passes the barrier). Re−do step 1 through 7 to check the correct latch−off trigger.

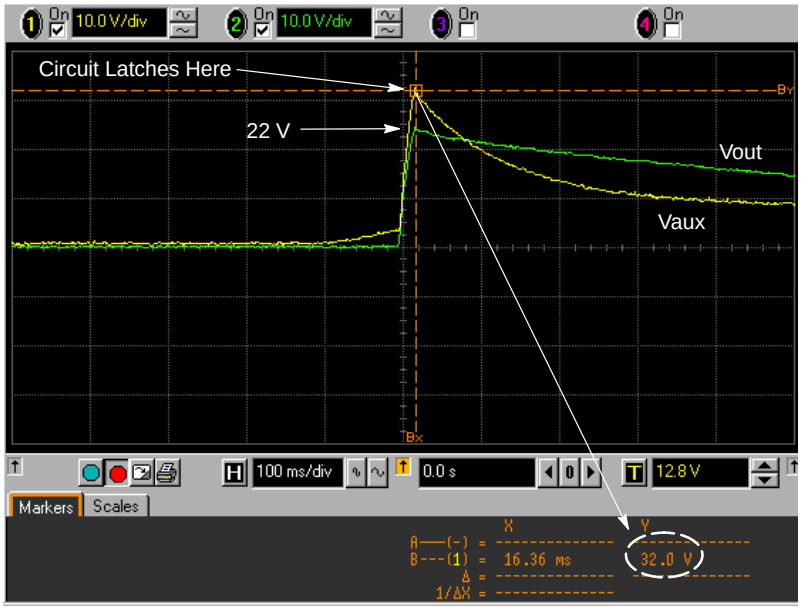

Figure 7. The circuit latches when Vaux grows−up to 32 V which corresponds to Vout = 22 V.

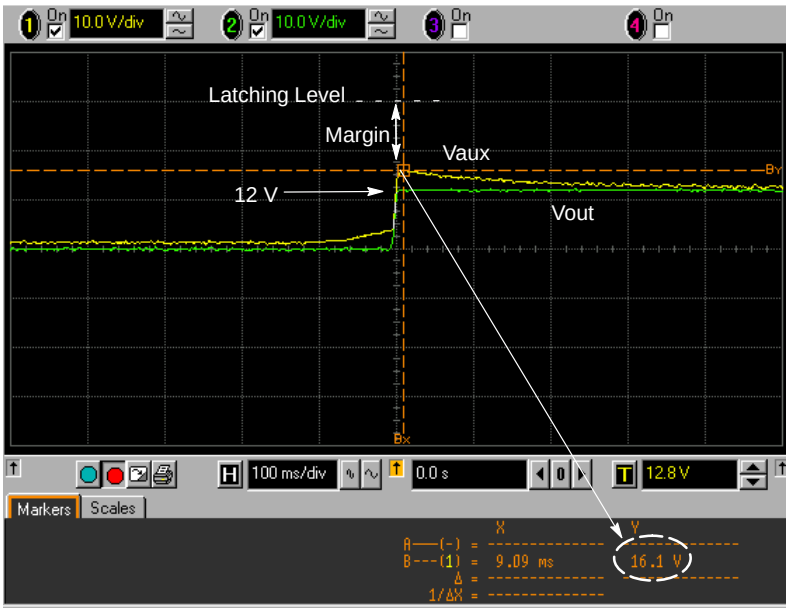

Figure 8. The selected resistor gives sufficient margin when Vout naturally overshoots on start−up.

Please note that this protective option is more to protect the converter and the load from a broken feedback loop operation rather than precisely clamp the output voltage with a precision of hundred of milli−volts.

Design Procedure with NCP101X, a Universal Mains Design, with DSS

Due to application note “Evaluating the Power Capability of NCP101X Members”, you have picked−up the right device, corresponding to the power level you want to reach with your supply. Suppose a NCP1013P06 has been selected from Table 6, e.g. a 350 mA 65 kHz device and you plan to build a 12 V−12 W adapter, operating at 50°C ambient, featuring the DSS, operated on European mains (230 VAC ± 15%):

1. The rectified bulk voltage will be: VinDC min = (230 – 15%) x 1.414 = 276 VDC, VinDC max = (230 + 15%) x 1.414 = 374 VDC.
2. As detailed in the data sheet, it is not possible to reflect a Flyback voltage greater than Vin, to avoid forward biasing the MOSFET body−diode. Also, care must be taken to not grow the drain voltage above its breakdown value, 700 V. Therefore, the turn−ratio will be bounded between two equations, the first being the BVdss, the second one limiting the reflected voltage to not forward bias the MOSFET body diode:

$$N \times (Vout + Vf) + VinDC\,max + Vleak \lll 700\ V \quad \text{(eq. 2)}$$

$$N \times (Vout + Vf) \lll VinDC\,min \quad \text{(eq. 3)}$$

With Vf, the secondary diode forward drop (0.5 V for a Schottky in our case), Vleak the leakage excursion (safely clamped by a RCD network) and N, the turn ratio Np/Ns. If we take 80 V for the leakage excursion (safety margin), then equation 2 gives a turn ratio of 20, whereas equation 3 gives a turn−ratio of 22. We will chose a value of 20, reflecting 20 x 12.5 = 250 VDC during the MOSFET *off* time. This respects equation 2 (MOSFET BVdss not reached) and also ensures that the valley of Vds(t) will not dip below ground during *off* time ringing.

3. Taking a ratio of 20, will guide us to select the right secondary diode. Its Peak Inverse Voltage (PIV) is defined by: (VinDC max/N) + Vout (eq. 4). This leads to a maximum reverse voltage of (374/20) + 12 = 30.7 V, applied when the primary MOSFET is *on*. A 40 V/3.0 A Schottky diode will perfectly fit in our design, e.g. an MBRA340.
4. As explained in the text, we will strive to keep the converter in Discontinuous Conduction Mode (DCM) with a duty−cycle less than 40% at VinDC min to offer a comfortable DSS operation. If we would not use the DSS, we could freely select the duty−cycle of choice as long as we respect the maximum value stated in the data−sheet. Keeping the supply in DCM is of good practice since, in that case, the turn−on losses are almost zero, if we neglect the capacitive losses. We will need a few equations to determine the primary inductance Lp but the method will slightly differ from what we are used to write. Here, several parameters are bounding the design such as the available peak current and the duty−cycle. Therefore, following the below lines will let you know if the original design parameters (power and voltage) are part compatible and end−up with a working converter:

a) From the application note “Evaluating the Power Capability of NCP101X Members” – Table 3, we know that the available peak current is actually the minimum of the specification, that is to say Ip_*selected* = 320 mA (in our case, the peak current is simply given by the minimum of the data sheet, rounded to 320 mA).

b) Calculate the critical inductance not to exceed in order to stay DCM given the design parameters:

$$Lp_{critical} = \frac{(VinDCmin \cdot Vr)^2 \cdot \eta}{2 \cdot Fsw \cdot [Pout \cdot (Vr^2 + 2 \cdot Vr \cdot VinDCmin + VinDCmin^2)]} \quad \text{(eq. 4)}$$

$$Lp\ critical = 8.8\ mH$$

c) Then evaluate the maximum value for the primary inductance since we are bounded by the duty−cycle max (maxDC = 40%) and the peak current:

$$Lpmax = \frac{DCmax \cdot VinDCmin \cdot Tsw}{Ip\_selected} = 5.3\ mH \quad \text{(eq. 5)}$$

d) check Lpmax < Lp critical given by eq. 4. This is okay.

e) check the maximum power you can get in DCM with Lpmax and Ip_*selected*:

$$Pout = \frac{1}{2} \cdot Lpmax \cdot Ip\_selected^2 \cdot Fsw \cdot \eta \quad \text{(eq. 6)}$$

→ Pout = 13.6 W, okay, greater than needed.

f) calculate the RCD clamping network, assuming a leakage inductance of 2% of Lp: 2% (5.3 mH) = 106 μH. Since we reflect 250 V, we will clamp at 300 V, limiting the drain excursion to 374 + 300 = 674 V < 700 V BVdss. The peak current worse case is now the maximum of the specification, therefore 350 mA + 10% = 385 mA. We can now apply the formulae for the RC element calculations:

$$Rclamp = \frac{2 \cdot Vclamp \cdot (Vclamp - Vout \cdot N)}{Lleak \cdot Ipmax^2 \cdot Fsw} \quad \text{(eq. 7)}$$

= 29 kΩ → 27 kΩ, P = 3.0 W

$$Cclamp = \frac{Vclamp}{Vripple \cdot Fsw \cdot Rclamp} \text{ (eq. 8)}$$, with

Vripple = 20 V, Cclamp = 7.8 nF → 22 nF

The diode can be an MUR160, an ultra−fast diode.

Checking the Design with Spice

A Spice simulator offers a way to check our design assumptions and see if they deliver the expected results. The model we made is available under both Intusoft's IsSpice and OrCAD's PSpice. The Flyback template appears in Figure 9, with our values plugged into the models. The secondary network is a TL431 whose bandwidth has been rolled−off via the 100 nF capacitor. Please note the presence of the leakage inductance and the calculated RCD clamp. If we missed the right values for this network, the library will not blow, this is the nice thing with simulation.

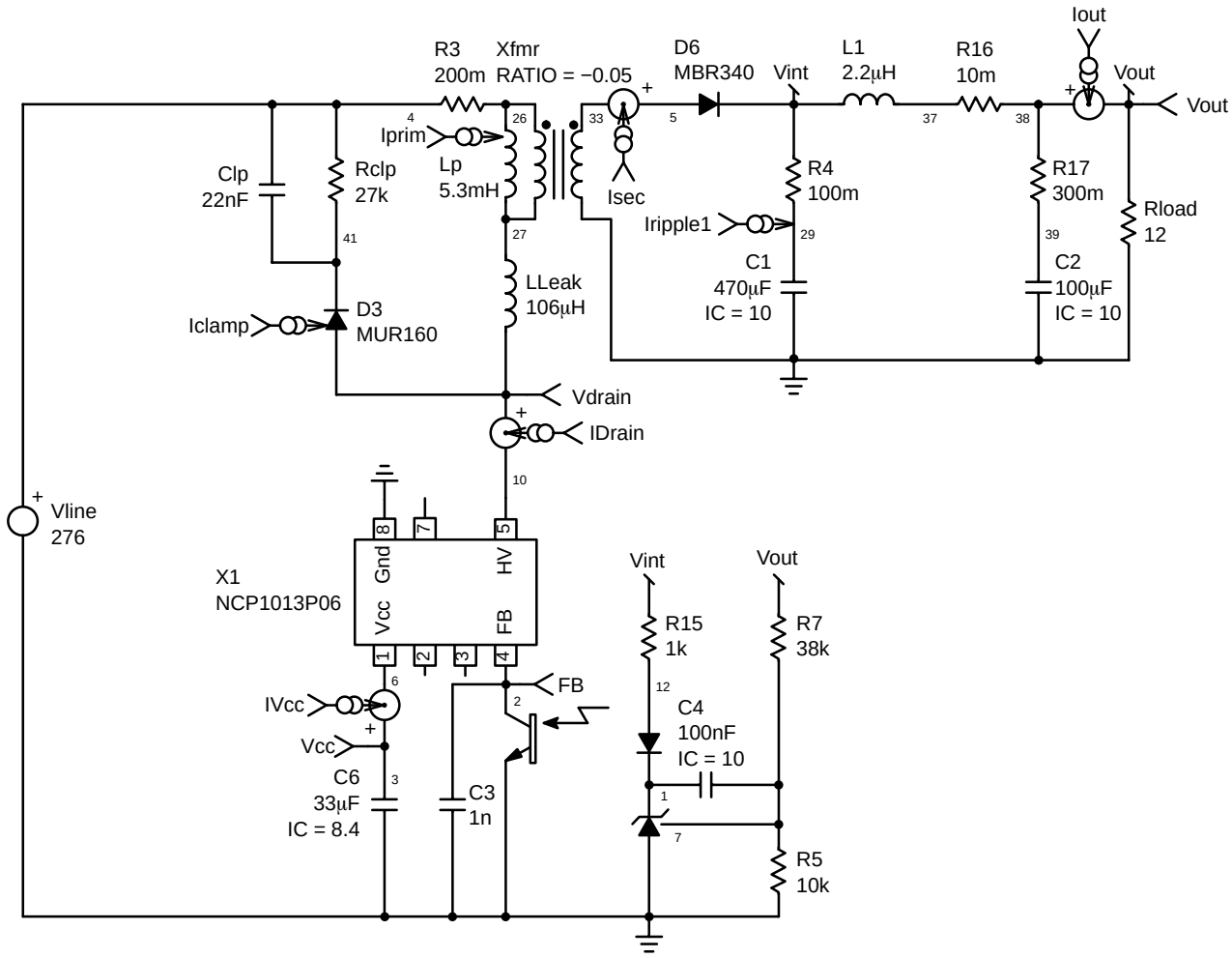

Figure 9. An IsSpice Simulation Template to Check the Design Validity

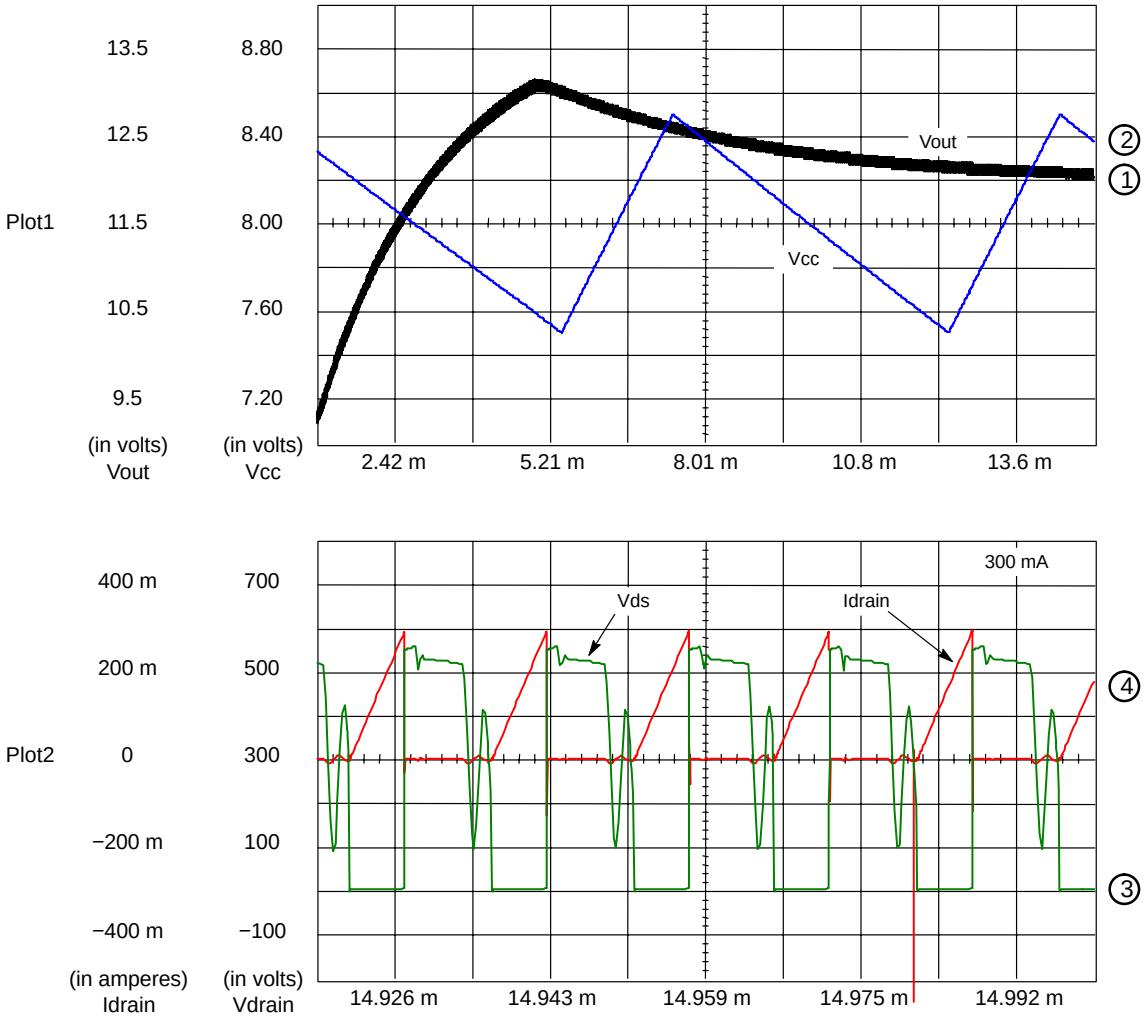

Figure 10. Results to Check Parameter Compliance

From Figure 10, we can see that low line confirms the 40% duty−cycle (Pout = 12 W) and the discontinuous operation. Different waveforms would reveal a good safety margin between Vds(t) and the 700 V BVdss.

Conclusion

This application note describes the design methodology of the NCP101X devices whose various features bring ease and speed of design. By following the steps, it becomes simple to develop and test with Spice, a power supply tailored to your needs.

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